FIG. 1

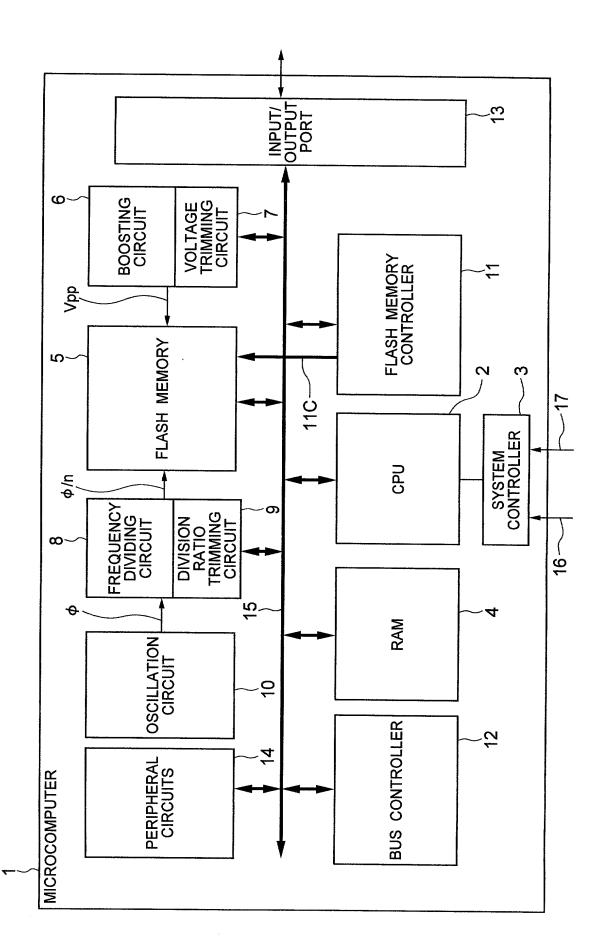


FIG. 2

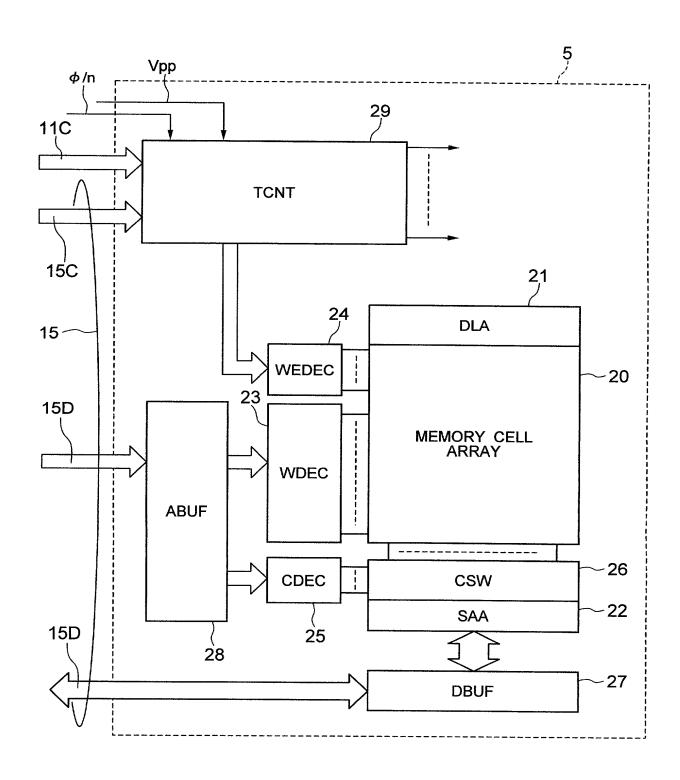
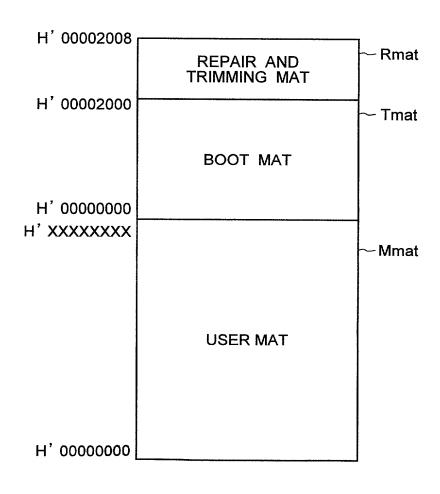


FIG. 3



EVALUATION DEVICE (TESTER) Vref Pad dd/ 13 PROGRAM EXECUTION -START CONTROL SIGNAL 62 DECISION REGISTER FIG. 4 63 RAM TRIMMING REGISTER DECODER **BOOSTING SECTION** 99 CPU REFERENCE VOLTAGE VOLTAGE GENERATION CONTROL REGISTER 65 64 FLASH MEMORY S - 09 61 <u>5</u>

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FIG. 5

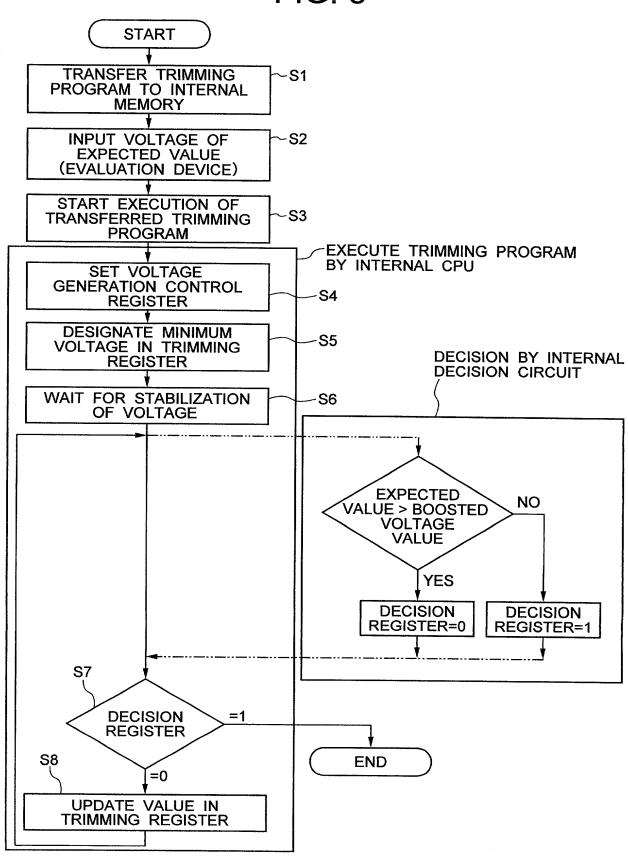
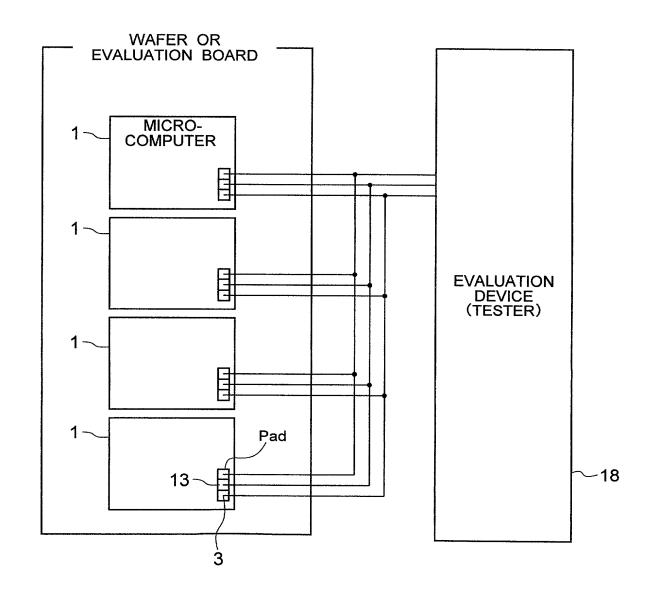
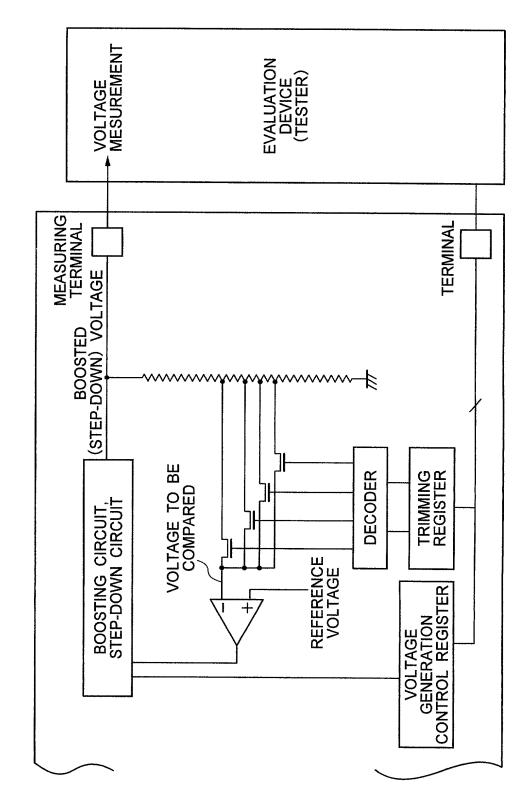


FIG. 6



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FIG. 7



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FIG. 8

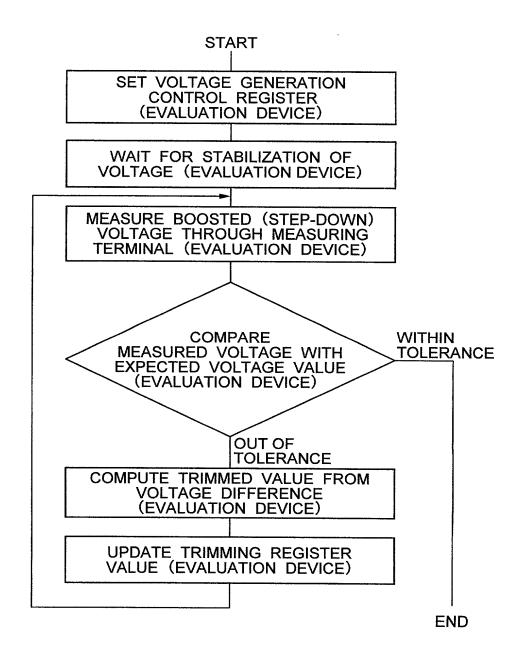


FIG. 9

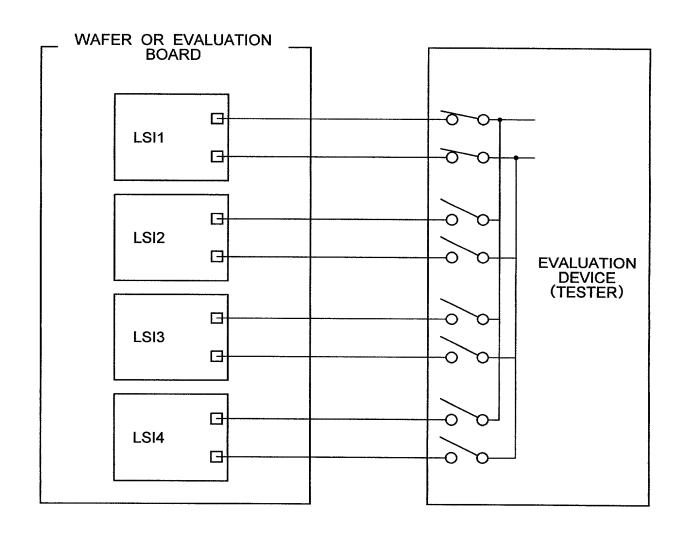
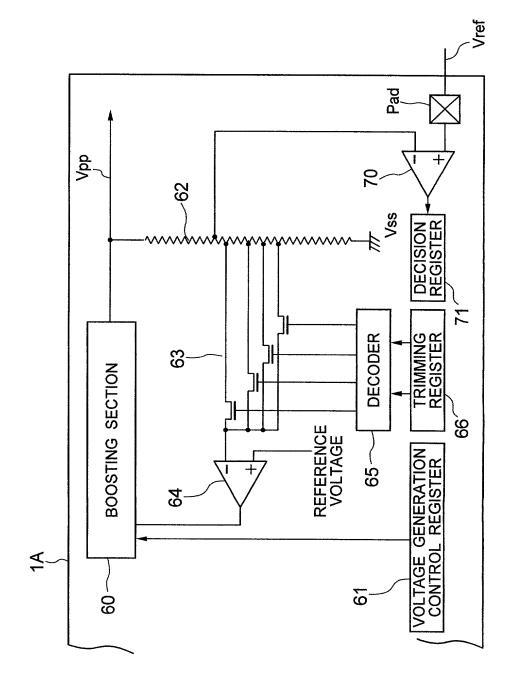
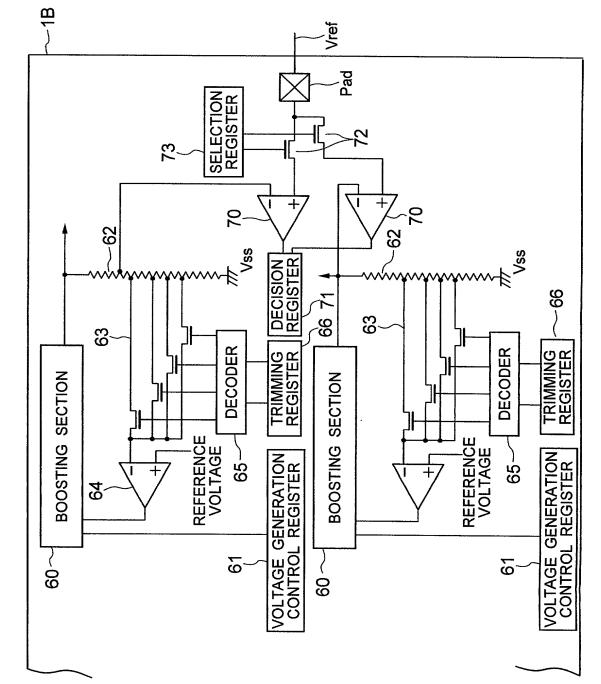


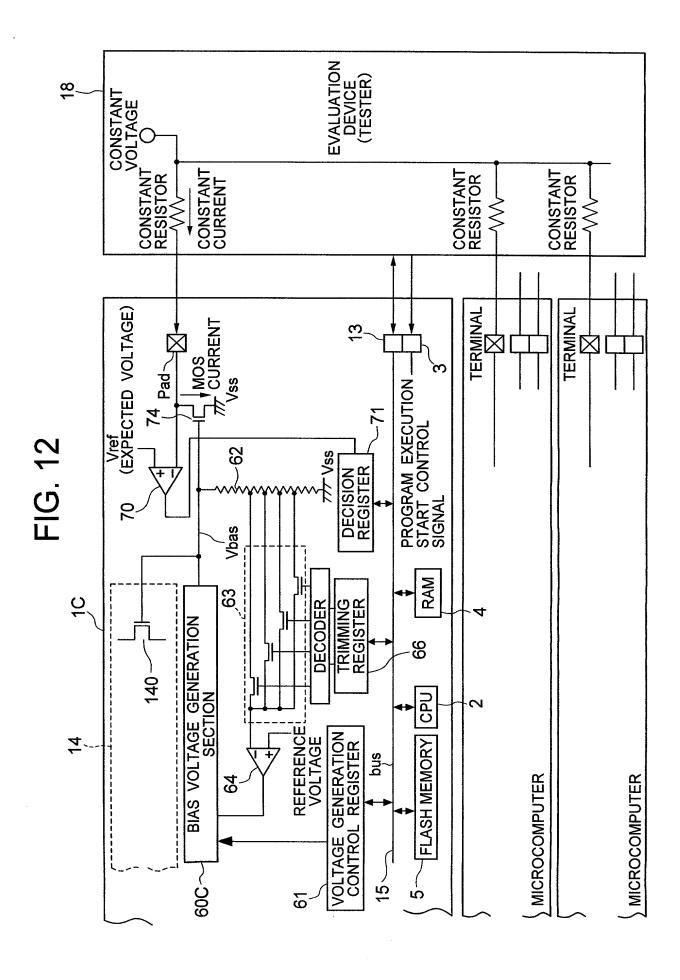
FIG. 10



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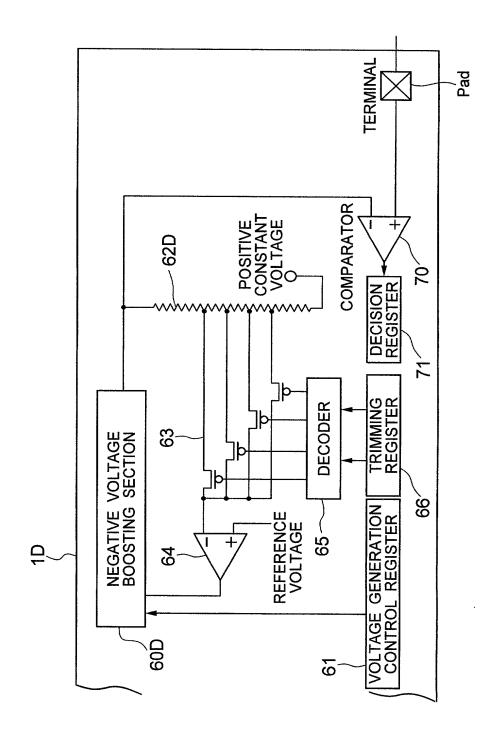
FIG. 11





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FIG. 13



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Pad Pad S POSITIVE SCONSTANT VOLTAGE -62D -62 DECISION REGISTER FIG. 14 9 63 63 TRIMMING REGISTER DECODER NEGATIVE VOLTAGE BOOSTING SECTION POSITIVE VOLTAGE BOOSTING SECTION REFERENCE VOLTAGE F REFERENCE VOLTAGE 65 VOLTAGE GENERATION CONTROL REGISTER 8 8 **~ □09** 61 ~ 09

NEGATIVE REFERENCE VOLTAGE POSITIVE REFERENCE VOLTAGE

99

TRIMMING REGISTER

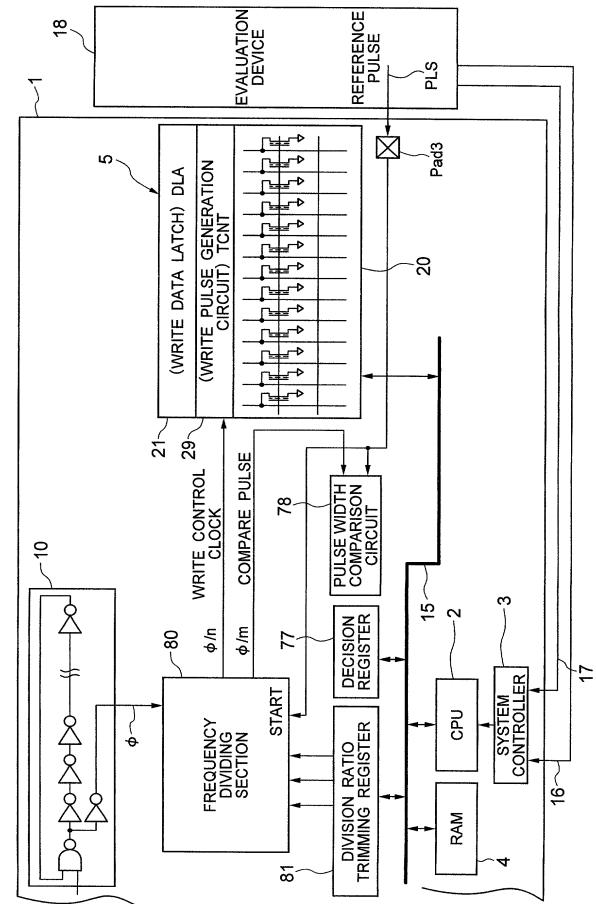
VOLTAGE GENERATION CONTROL REGISTER

DECODER

65

6

FIG. 15



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FIG. 16

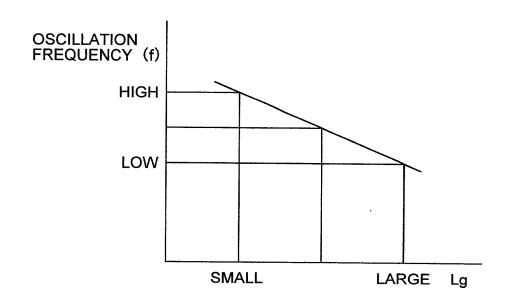
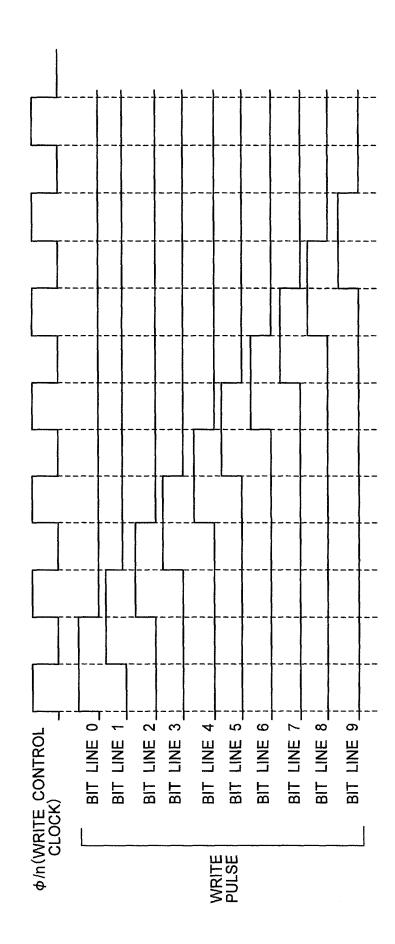
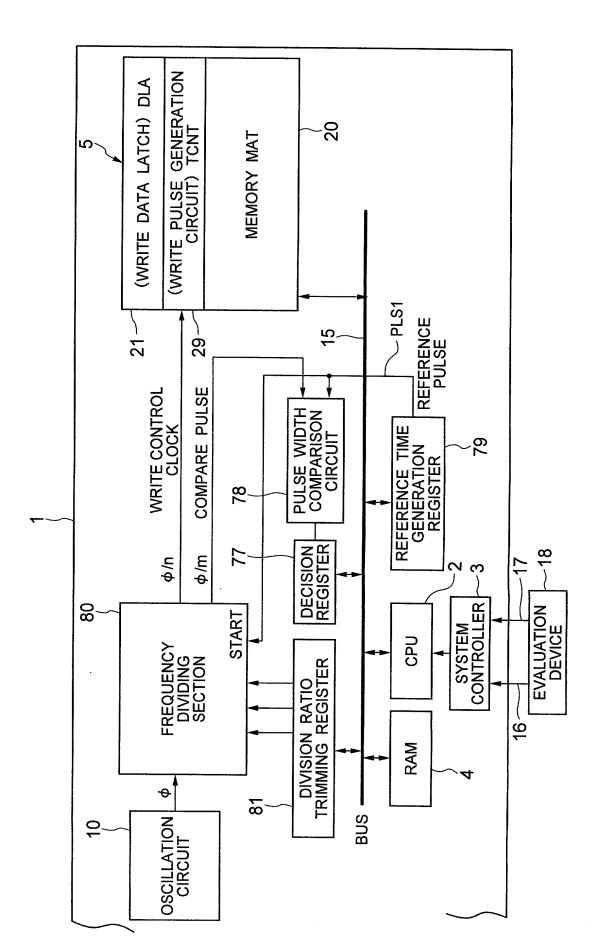


FIG. 17



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FIG. 18



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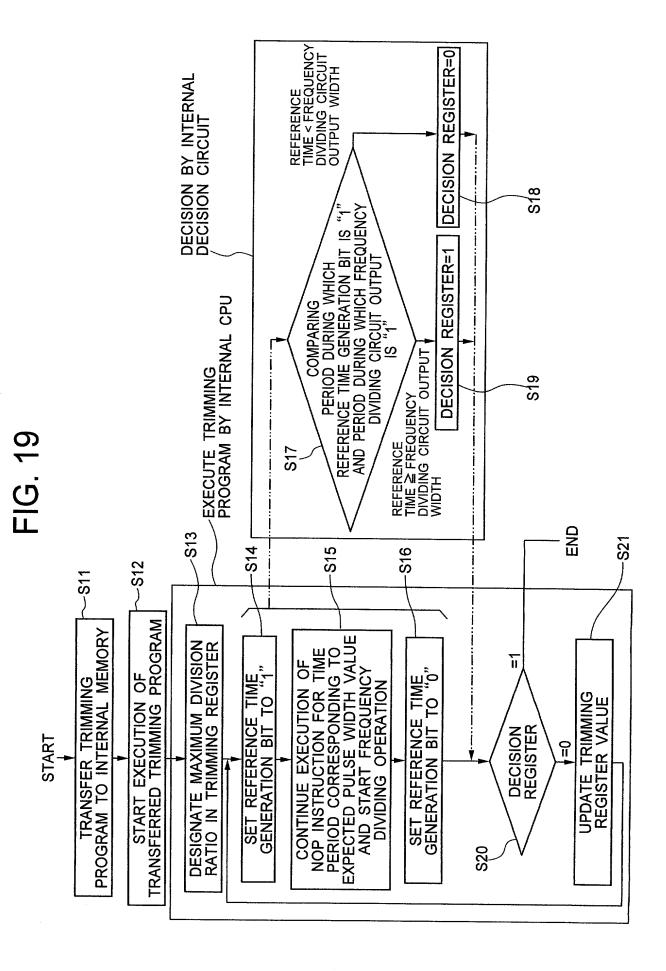


FIG. 20

		Γ			T	<u> </u>	Τ	<u> </u>	
TRIMMING	FREQUENCY (\$\phi\) AFTER TRIMMING	64/64=1.0MHz	60/60=1.0MHz	56/56=1.0MHz	52/52=1.0MHz	48/48=1.0MHz	44/44=1.0MHz	40/40=1.0MHz	36/36=1.0MHz
	DIVISION RATIO	1/64	1/60	1/56	1/52	1/48	1/44	1/40	1/36
	TRIMMING REGISTER	(0,0,0)	(0,0,1)	(0,1,0)	(0,1,1)	(1,0,0)	(1,0,1)	(1,1,0)	(1,1,1)
RING OSCILLATOR FREQUENCY		64MHz	60MHz	56MHz	52MHz	48MHz	44MHz	40MHz	36MHz

FIG. 21A

<TRIMMING REGISTER=(0,0,0)> MAXIMUM DIVISION RATIO IS DESIGNATED

IN TRIMMING REGISTER

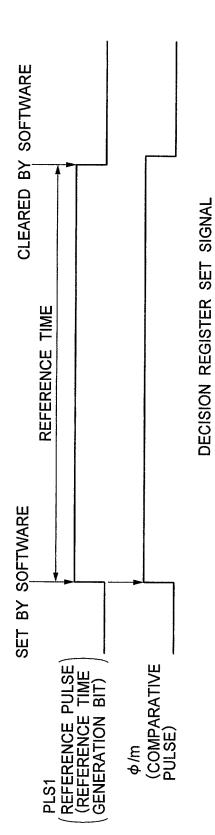
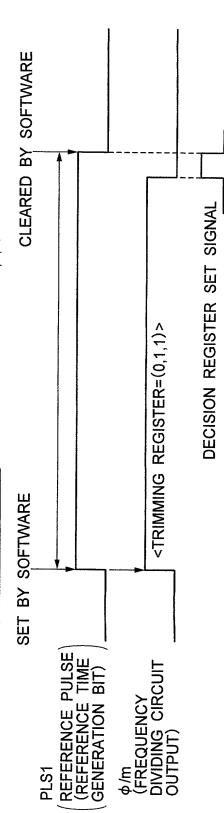


FIG. 21B

VALUE IN TRIMMING REGISTER IS UPDATED <TRIMMING REGISTER=(0,1,1)>



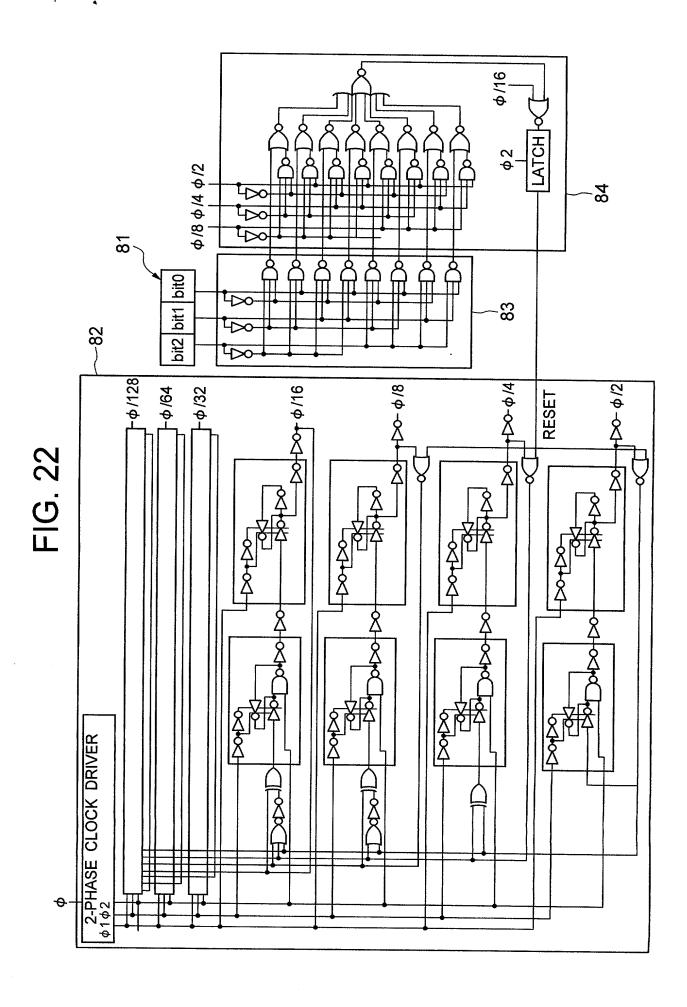
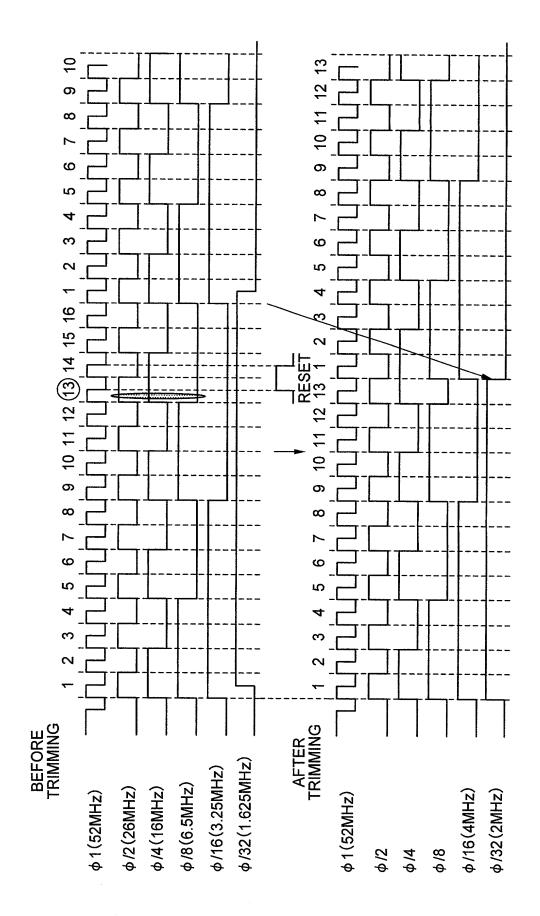


FIG. 23



S F

FIG. 24

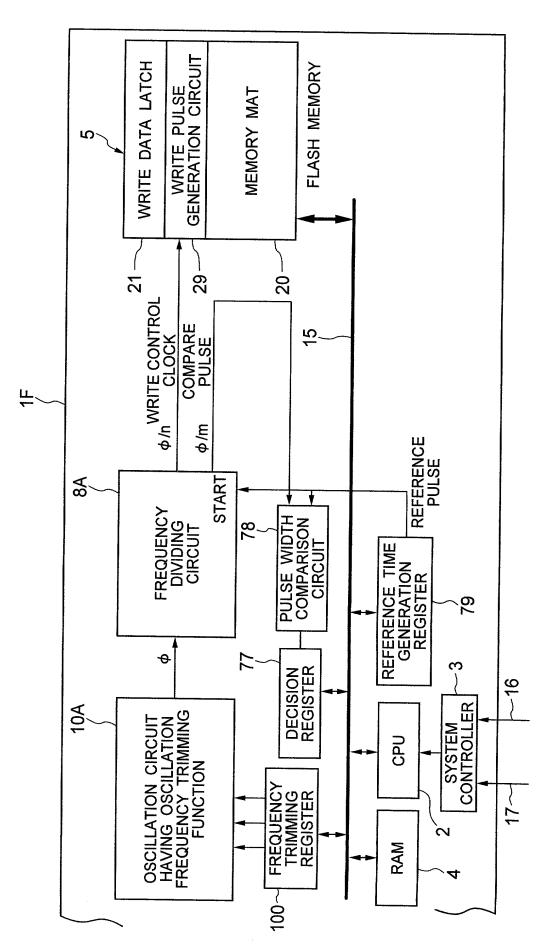
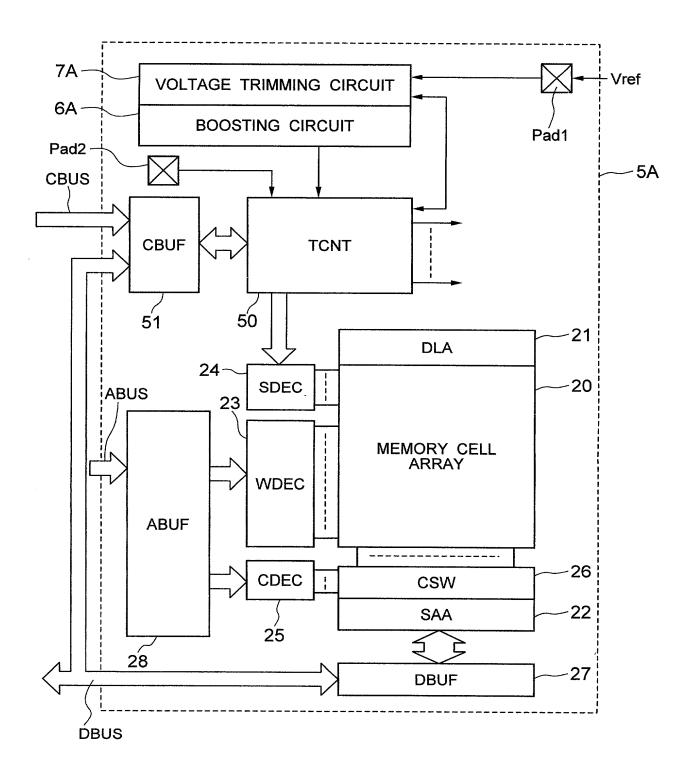


FIG. 25



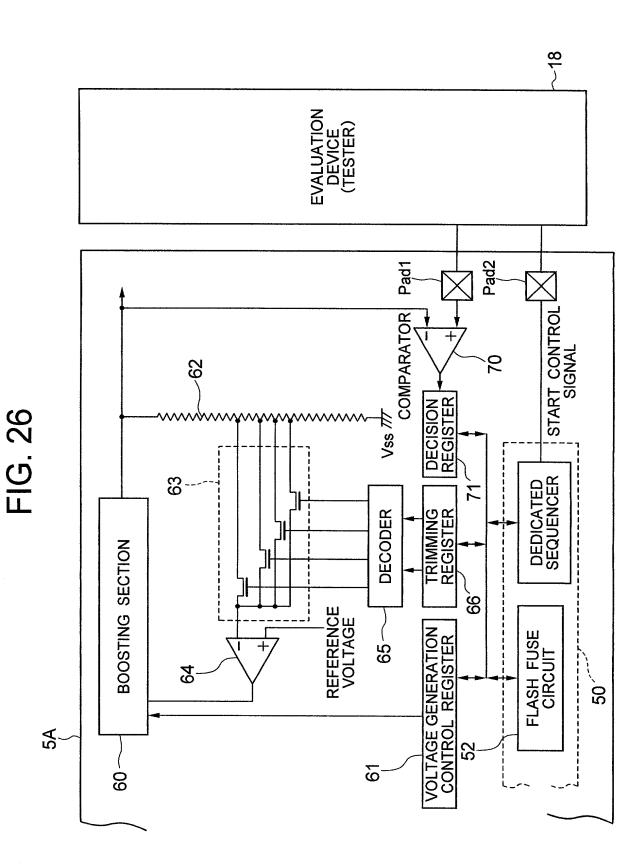
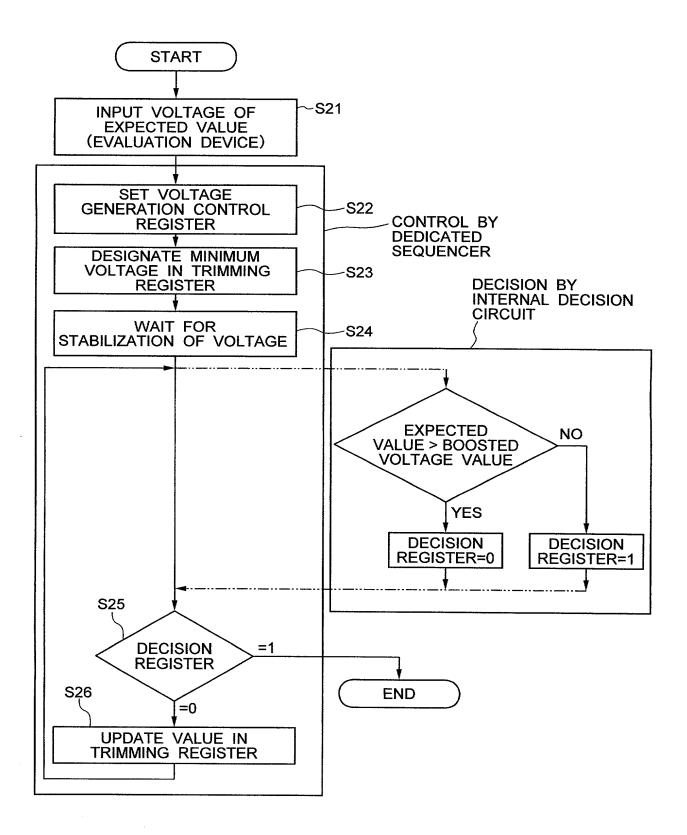


FIG. 27



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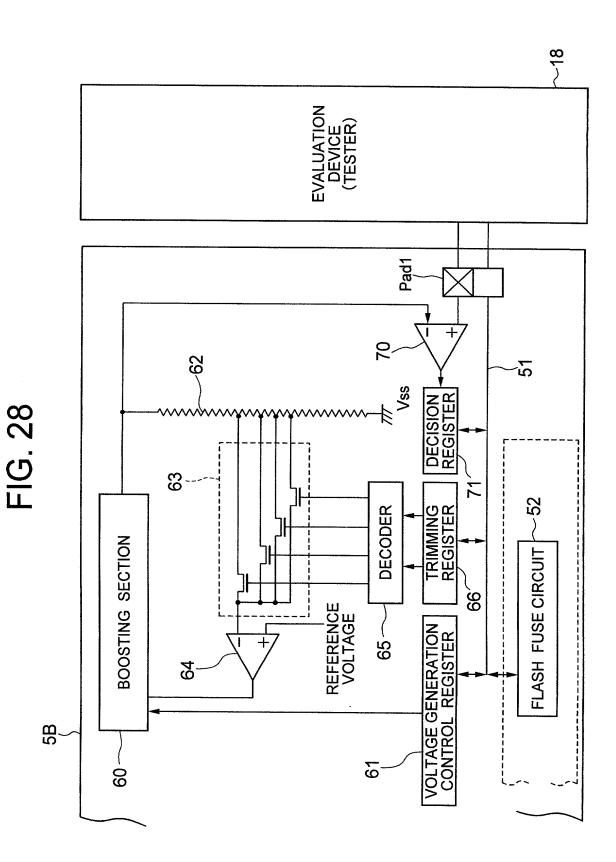


FIG. 29

